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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,035	03/15/2004	Jun Koyama	12732-218001 / US7081	6874

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EXAMINER	
CRANE, SARA W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,035	KOYAMA, JUN	
	Examiner	Art Unit	
	Sara W. Crane	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *21,22,24,26 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20, 23, 25, 27, 28, 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan et al.

The reference is drawn to an adaptive power supply for digital integrated circuits (column 1, line 26). Transistors of the circuit may be fabricated on an SOI wafer (column 7, line 28), which would be a substrate having an insulating surface. Logic circuits are encompassed by the teaching, or, alternatively, obvious in view of the teaching, because microprocessors are mentioned specifically as exemplary (column 1, lines 43-45), and microprocessors incorporate digital logic circuits. Column 8, lines 57-48, teaches that a control loop selects a substrate bias voltage in correspondence to present frequency data. A "detection means" for detecting the operating frequency would have been obvious, because such a means would have been necessary to determine the present frequency data giving the present operating frequency of the circuit. The substrate bias voltage is for the purpose of controlling threshold (paragraph spanning columns 2 and 3, column 7, lines 29-31).

Claims 1-20, 25, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan et al. in view of Skotnicki et al.

With respect to claim 1, the limitations of lines 1-4 would be as discussed above with respect to the Chandrakasan reference. Column 7, lines 29-31, of this reference notes the use of a buried gate structure for threshold value control of a transistor. A second gate, other than the buried gate, would be inherent, or alternatively obvious, because in order to be useful the transistor would be expected to respond to an input signal as well as the threshold bias. Skotnicki et al. teaches an example of a thin film transistor having a buried gate 2 and a second gate 10 (column 4, lines 55-60). It would have been obvious to incorporate a transistor such as that of Skotnicki in the Chandrakasan circuitry, in order to provide for both signal input and threshold bias control.

With respect to claim 2, the Skotnicki device has the recited structure. With respect to claim 3, in would have been obvious to provide a CPU, which must include logic, with the detection means necessarily to implement the Chandrakasan biasing, to obtain the low power processor as desired in that reference. With respect to claims 4-5, the use of the Chandrakasan power reduction would have been advantageous in circuits implementing any of the uses listed. With respect to claim 6, controlling the amount of current flow between source and drain is the function of any gate, particularly a gate that controls threshold voltage, and this function would therefore have been inherent, or alternatively obvious, in the Skotnicki transistor. With respect to claim 11, Chandrakasan column 8, lines 55-58, teaches that there is a look-up table recording the

present frequency data, so there must be some sort of "recording medium" storing the table information. Column 8, lines 35-38, teaches that a control algorithm may be implement in software, firmware, or hardware. A control algorithm would be a program, which, as noted in lines 55-58, has as output a bias voltage for threshold control. Other claim limitations not specifically discussed above, parallel those which are discussed, and would have been taught, or obvious, for the same reasons.

Claims 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan et al. and Skotnicki et al, as discussed above, and further in view of Yamagishi.

Yamagishi teaches column 3, lines 50, through column 4, line 5, a frequency detection circuit having a counter 40 and a discrimination circuit 41. The output of the discriminator selects one of n switches. An address comparator would have been obvious as part of the discriminator in order to determine which switch to select. It would have been obvious to use a frequency detection circuit as taught by Yamagashi to determine frequency as needed for the Chandrakasan threshold biasing, in order to determine operating frequency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.

The supervisor for Art Unit 2811, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara W. Crane
Primary Examiner
Art Unit 2811